VXI-5524A

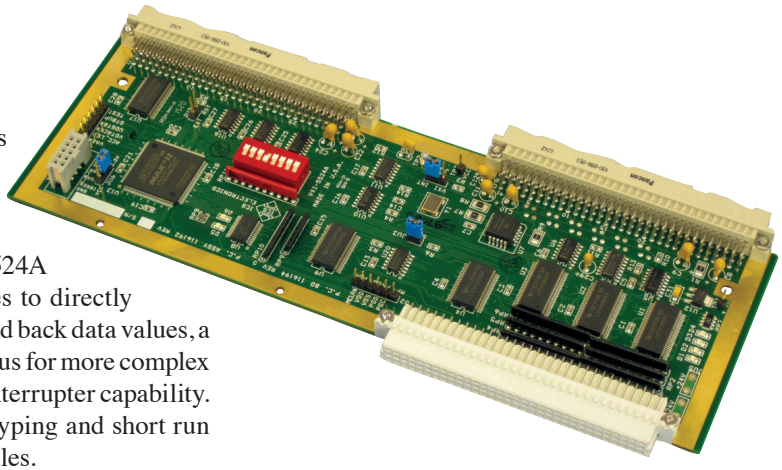
VXI INTERFACE CARD

"The fastest way to build a VXI Module"

- Mates with user's PCB to form a C or B-size module. *The quickest way to make a VXI module.*
- Provides 48 latched I/O signals, a VXI expansion bus, TTL Triggers and VXI interrupt capability. *Supports virtually any kind of user circuit or function.*
- 3.3V, 5 V tolerant Digital IO and VXIbus signals *Easily used with 3.3V circuits without level conversion.*
- User configurable model number, manufacturer ID, version and serial numbers *Identifies the finished module as your product.*
- Two companion component boards available for prototype modules *No need to layout prototype boards.*
- Module hardware kits available for building 1, 2 or 3-slot wide modules. *Complete hardware support for C-size modules.*
- VXI-1 Rev 4.0 and VXI-2 compliant register-based interface.
  High speed VXIbus interface that meets the latest VXIbus specifications

DESCRIPTION

ICS's Model VXI-5524A is a low-cost VXI Register Interface for connecting virtually any kind of a circuit to the VXIbus. The VXI-5524A provides 48 digital I/O lines to directly control simple circuits or read back data values, a 16-bit VXI data expansion bus for more complex circuitry plus triggers and interrupter capability. Applications include prototyping and short run VXIbus C and B size modules.



VXI-5524A Interface Board

Packaging Concept

The VXI-5524A interface is a narrow PC card that is located at the VXI bus end of the module. The user places his components on a separate printed circuit board which mates with the VXI-5524A to make a complete 'B' or 'C" size assembly. The two cards mate together with a right-angle 96-pin DIN connector and are mechanically held together with a metal bracket.

For quick prototyping, ICS offers a companion sea-of-holes board with holes on 0.1 inch centers and a bare copper clad board. ICS also supplies design kits and CAD templates so the user can layout his own printed circuit board.

The VXI-5524A can be enclosed with ICS's 11434x series VXI Hardware Kits to make a complete 1, 2, or 3-slot wide module. Each VXI Hardware Kit includes a blank front panel, side shields and all the hardware necessary to make a complete 'C' size Module.

User's Interface

The VXI-5524A's user interface includes 48 static digital lines, a VXI data expansion bus, TTL trigger lines and VXIbus interrupt lines. The static digital interface has three 16-bit registers that can be configured as latched outputs to control the user's circuits or as gated inputs to read back data or signals. The expansion bus is a buffered, 16-bit wide VXI D16 data bus with address capability to read and write to 26 additional registers.

The user interface also has a two trigger lines that connect to a selected pair of the VXIbus TTL Trigger Lines. The input trigger can be used to start an event on the user's circuit. The output trigger line can be used to drive the VXIbus TTL Trigger line and trigger other VXI modules. The user interface has an interrupt line that can be pulsed to generate a VXIbus interrupt on a selected VXI IRQ line. The VXI-5524A reports three bits for 8 interrupt codes as part of the interrupt response word.

The user interface also includes a 10 MHz clock and all seven VXIbus voltages.

Easy Configurability

All of the VXI-5524A's configurable functions, such as the manufacturer ID code and model number, serial number, etc. are stored in a nonvolatile EEPROM and are restored when the card is reset or powered on. The user sets the configurable parameters to personalize the finished VXI module as his product.

Register Based Interface Advantages

Data transfer time can limit a module's performance regardless of how good the rest of the circuits are. Message based modules provide the intelligence and flexibility of a on-board processor but are limited by the slow data transfer rate of the VXIbus word serial transfer protocol. VXI-5524A Register based modules are not limited by the word serial protocol as each data register is directly addressable by the VXIbus controller. Command interpretation is done in the user's logic or by the device driver in the Bus controller which further speeds up the module's response.

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VXI-5524A Block Diagram

A block diagram of the VXI-5524A is shown in Figure 1 on the right. It shows the 48 bidirectional digital I/O lines, an expansion bus for driving additional circuits, address and strobe lines, VXI triggers, interrupt inputs, power and clocks. This selection of signals makes it very easy for the user to build virtually any kind of a circuit on the mating board. Simple circuits with minimal data needs can be driven directly from the 48 data lines without any additional logic. More complex circuits such as data converters, FIFOs etc. or circuits that need additional I/O lines can be attached to the buffered expansion bus.

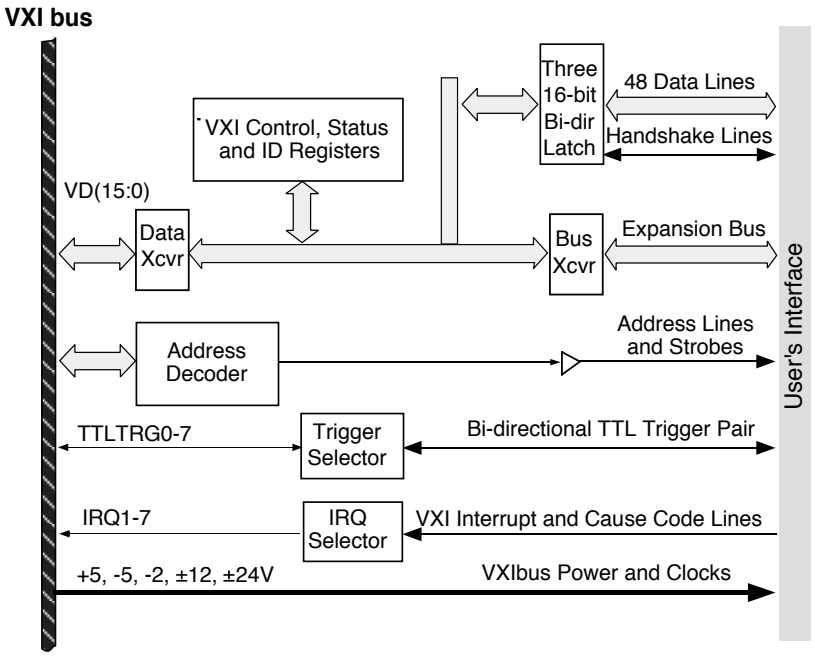

Figure 1 VXI-5524A Block Diagram

Data Lines

Up to 48 data lines can be controlled by addressing the three bidirectional latches on the VXI-5524A. The latch direction is set by bits in the Control Register. When configured as outputs, the latches hold data to drive the user's circuits. The latch outputs are high current drivers capable of sinking 64 mA and sourcing 24 mA. When configured as inputs, the latches are open circuit inputs with pullups to 3.3 Vdc for inputting data from TTL, CMOS or contact closures. When more than 48 data lines are needed, additional latches or other circuits can be placed on the user's circuit board and attached to the VXI data expansion bus.

The data expansion bus is a 16-bit wide bus that buffers the VXI D16 data lines onto the user's circuit board. Handshake lines include an address select strobe, a write line and a not-ready line to hold the VXI DTACK line while the data is being read.

Register Addressing

All VXI modules are assigned 64 bytes or thirty-two 16-bit word addresses in the A16 address space. The VXI-5524A uses the first sixteen addresses, 00 hex to 1F hex, for its VXI registers and for compliance with the new VXI Specification for Extended Register Based Devices. Addresses 3A-3E hex are used for the 48 data I/O lines. Addresses, 20 hex to 38 hex, are encoded on 4 address lines for the user's logic so they can be easily decoded with a '138' type decoder to address additional devices.

Trigger and IRQ Lines

The VXI-5524A's Trigger Selection logic selects a pair of adjacent VXI TTLTRG lines and routes them to the user's circuit board. The lower TTLTRG line is an input trigger to initiate action on the user's circuit. The higher TTLTRG line drives a VXIbus TTL Trigger line to trigger other modules.

The VXI-5524A's IRQ Selection logic routes a user interrupt onto one of the 7 VXIbus IRQ lines. When the user's logic pulses the IRQ line, the VXI-5524A latches a 3-bit cause code for use in the Interrupt Response word and for the VXI-2 Interrupt Status Register.

Clock and Power

A clock signal and all VXI voltages are routed to the user's interface connector. A jumper on the VXI-5524A lets the user select the VXI-5524A's 10 MHz oscillator or the VXIbus CLK10 signal as the module's clock source.

PCB Layout Aids

ICS provides drawings and CAD design aids to simplify the design of the user's mating PC board to the VXI-5524A. The mating board outline drawing and suggested bill of materials are part of the VXI-5524A's Instruction Manual.

PCB design files and CAD templates are also available on a CD-ROM. These design aids include the board outline drawings, parts library and a prototype schematic. The CAD files are supplied as DXF files and in ORCAD design format. Both file formats are compatible with most PC layout and schematic capture systems. The prototype schematic includes all of the signals on the user interface. To complete the design, the user just has to add his components to the schematic and route the final design.

Complementary CD-ROMs (Part number 123153) are available at no charge to any qualified VXI designer or customer. Call for your copy or email sales@icselect.com with your name, company name and mailing address.

TABLE 1
USER INTERFACE SIGNAL-PIN ASSIGNMENTS

Pin	Signal	Pin	Signal	Pin	Signal
A1	Inhibit#	B1	Cause1	C1	+ 12 V
A2	Clk10	B2	Cause2	C2	- 12 V
A3	NRdy#	B3	Cause3/RST#	C3	- 2 V
A4	Clear#	B4	EDR#	C4	- 5.2 V
A5	Strobe#	B5	Vcc	C5	Vcc
A6	DWrite#	B6	Gnd	C6	Gnd
A7	DStb#	B7	D15	C7	D7
A8	IRQ#	B8	D14	C8	D6
A9	TrigOut#	B9	D13	C9	D5
A10	TrigIn#	B10	D12	C10	D4
A11	A1	B11	D11	C11	D3
A12	A2	B12	D10	C12	D2
A13	A3	B13	D9	C13	D1
A14	A4	B14	D8	C14	D0
A15	CH48	B15	CH40	C15	CH32
A16	CH47	B16	CH39	C16	CH31
A17	CH46	B17	CH38	C17	CH30
A18	CH45	B18	CH37	C18	CH29
A19	CH44	B19	CH36	C19	CH28
A20	CH43	B20	CH35	C20	CH27
A21	CH42	B21	CH34	C21	CH26
A22	CH41	B22	CH33	C22	CH25
A23	CH24	B23	CH16	C23	CH8
A24	CH23	B24	CH15	C24	CH7
A25	CH22	B25	CH14	C25	CH6
A26	CH21	B26	CH13	C26	CH5
A27	CH20	B27	CH12	C27	CH4
A28	CH19	B28	CH11	C28	CH3
A29	CH18	B29	CH10	C29	CH2
A30	CH17	B30	CH9	C30	CH1
A31	Acc_LED#	B31	SysFail_LED#	C31	+ 24 V
A32	Rdy_LED#	B32	Fail_LED#	C32	- 24 V

Notes:

1. # indicates low true signal.

TABLE 2
SIGNAL DEFINITIONS

Signal	Definition
A(1:4)	Data Bus address lines for VXI register addresses 20-3A HEX.
Acc_LED#	Drives Access LED on user's board.
Cause1	User IRQ cause bit 1 (LSB)
Cause2	User IRQ cause bit 2
Cause3/RST#	Dual purpose line. If VXI-5524A reset jumper is not installed, the line is the IRQ cause bit 3. If the reset jumper is installed, the line used to reset the VXI-5524A board logic.
CH(1:48)	Data IO lines. Data direction set in 16 line increments by user configuration.
Clear#	Clear strobe to reset user's circuits.
Clk10	10 MHz clock. VXIbus CLK10 or VXI-5524A 10 MHz oscillator.
D(0:15)	VXI Expansion Data Bus, D0 is LSB
DStb#	Data Bus transfer strobe. Asserted when Expansion Bus addressed.
DWrite#	Data Bus Write direction line. Asserted when VXIbus is writing data.
EDR#	External Data Ready input for handshaking CH input lines. User sets EDR F/F when data is ready.
Fail_LED#	Drives Failed LED on user's board.
Inhibit#	Inhibit signal from EDR flip-flop. Digital inputs should be held steady while Inhibit# is asserted.
IRQ#	User generated VXIbus interrupt. Latches Cause lines for interrupt response word.
NRdy#	User hold input holds VXIbus data transfer if NRdy# is low before DataStb# goes high.
Rdy_LED#	Drives Ready LED on user's board.
Strobe#	Transfer strobe when CH output data is stable.
SysFail_LED#	Drives SysFail LED on user's board.
TrgIn#	Selected TTL Trigger input line to user circuits.
TrgOut#	Trigger output line drives selected VXI-bus TTL Trigger line.

VXI-5524A: SPECIFICATIONS

VXI Specifications

VXI Capabilities

VXI-1 Revision 1.4 compliant
VXI-2 Revision 1.0 compliant
Static and Dynamic address capability
Register based
Servant device
A16 Address space, D16 Data
Programmable interrupter
Normal handshake data transfer
Includes VXI-2 Version, Serial Number, Interrupt and Subclass Registers.

Diagnostic Capability

Power-on self test
Built-in diagnostic routines
Four LEDs for VXI status and troubleshooting.

Indicators

Four LEDs showing the state of the VXIbus interface and VXI-5524A's logic.

RDY	On after self test
ACCESS	On when address recognized
FAIL	On when self test failed
SYSFAIL	VXIbus SysFail signal line

User Interface

Digital IO Lines

48 TTL data lines with 33 kohm pullups, organized as three 16-bit registers. Use as latched outputs or gated inputs for sensing TTL/CMOS/contact inputs. Control lines include input handshake lines and output data strobe.

Input Levels	High: >=2.4 Vdc or open circuit Low: < 0.6 Vdc at 200 µA
Output Levels	High: > 2.4 Vdc with - 8 mA source > 2.0 Vdc with -24 mA source Low: < 0.55 Vdc with 64 mA sink

Expansion bus

16 data lines, 4 address lines, strobe and write lines. Bus address range is 20 to 38 HEX. Signal levels same as Digital IO Lines.

Triggers

VXI TTLTRG lines selected in pairs.

TTL trigger input	Pulse waveform same as the VXIbus TTLTRG line 0, 2, 4, or 6. High: > 2.4 Vdc, -24 mA Low: < 0.55 Vdc, 24 mA
TTL trigger output:	Drives VXIbus TTLTRG line 1, 3, 5, or 7.

Interrupter Capability

Interrupter line and three Cause Code lines. Generates VXIbus interrupt and latches the cause code when the interrupter line is pulsed.

Other Signals

Clear#:	low true pulse to reset user logic. Signal levels same as Digital IO
RST#:	low true input to reset VXI-5524A.
Clk10:	VXIbus or VXI-5524A 10 MHz clock. Signal levels same as Digital IO Lines
LEDs	Low drive signals for operating front panel LEDs. High open collector, 5 Vdc pullups Low: <0.55 Vdc, 20 mA sink

Physical

Size, W x H x D

B/C-size narrow
9.187in W x 0.62 in H x 3.0 in D
(233 mm W x 15.7 mm H x 76.2 mm D)

Weight

0.14 kg. (0.32 lbs.)

Power interface logic uses:

5 Vdc @ 150 mA
-5.2 Vdc at 45 mA
-2 Vdc at 9 mA

User Interface

A 3 row x 32 pin DIN connector with the signals listed in Table 1.

VXI Interface

Standard P1 and P2 connectors.

Included Accessories

Instruction manual with PCB layout drawings, design rules for user's PCB and example user circuits.

Programming guide and sample routines for user interface signals, and expansion bus data transfers.

Mounting bracket.

Available Component Boards

Two boards with mating connector, front panel LEDs and Reset button. Prototyping Board has four power planes and holes on 0.1 inch centers. Bare board has copper-clad on both sides.

Available VXI Kits

Single, dual and triple wide C-size module hardware kits. Each kit includes side shields, blank front panels and all necessary hardware. Refer to ICS's VXI-KIT data sheets for more information about the 11434x and 114750 hardware kits.

ORDERING INFORMATION

	Part Number
VXIbus Register-based Interface Adapter Card with and mounting bracket	VXI-5524A
Protoype User Board with holes	114820
Prototype User Bare Board (Copper clad)	114830
VXIbus Hardware Kits	see separate data sheet